1. A non-volatile memory array, comprising:

a plurality of memory cells, each cell receiving a bit line, word line, and release line;

each memory cell including a cell selection transistor with first, second and third nodes, the first and second nodes being in respective electrical communication with the bit line and the word line,

each cell further including an electromechanically deflectable switch, having a first, second and third node, the first node being in electrical communication with the release line, and a third node being in electrical communication with the third node of the cell selection transistor, the electromechanically deflectable switch including a nanotube switching element physically positioned between the first and third nodes of the switch and in electrical communication with the second node of the switch and wherein the second node of the switch is in communication with a reference signal;

wherein each nanotube switching element is deflectable into contact with the third node of the switch in response to signals at the first and second node of the cell selection transistor and is releasable from such contact in response to a signal at the release line.

2. The memory array according to claim 1, wherein the cell selection transistor is a FET and the second node of the transistor is a gate of the FET.

3. The memory array according to claim 1, wherein the nanotube switching element is a ribbon of nanotube fabric.

4. The memory array according to claim 3, wherein each ribbon of nanotube fabric includes a plurality of carbon nanotubes.

5. The memory array of claim 3 wherein the nanotube fabric is porous.

6. The memory array of claim 3 wherein the nanotube fabric is substantially a monolayer of carbon nanotubes.

7. The memory array of claim 3 wherein the nanotube fabric is formed of single-walled carbon nanotubes.

8. The memory array of claim 1 wherein informational state of a memory cell is manifested by the position of the nanotube switching element and wherein the position of the nanotube switching element is sensed on the bit line as a time variation of the bit line signal.

9. The memory array of claim 1 wherein the release line is shared among a plurality of memory cells and wherein activation of the release line causes all nanotube switching elements of the plurality of memory cells sharing the release line to release from contact with a corresponding third node of the switch.

10. The memory array according to claim 2, wherein the FET is an NFET.

11. The memory array according to claim 2, wherein the FET is a PFET.

12. A non-volatile memory array, comprising:

a plurality of memory cells, each cell receiving a bit line, word line, and release line;

each memory cell including a cell selection circuit with first, second and third nodes, the first and second nodes being in respective electrical communication with the bit line and the word line,

each cell further including an electromechanical switch, having a nanotube switching element that is electromechanically deflectable into and out of contact with the third node of the

cell selection circuit, said nanotube switching element being in electrical communication with a reference signal.